上海贝岭 SHANGHAI BELLING

BL8082

PMU with 1 Synchronous Buck and 2 LDOs

DESCRIPTION

The BL8082 is a power management unit (PMU), with 1 synchronous Buck and 2 low-dropout regulators that delivers a maximum current of 1A for each individual output.

The synchronous buck is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 1.2A of output current. The device operates from an input voltage range of 2.6V to 7V and provides an output voltage from 0.6V to VIN, making the buck ideal for low voltage power conversions. Running at a fixed frequency of 1.5MHz allows the use of small external components, such as ceramic input and output caps, as well as small inductors, while still providing low output ripples. This low noise output along with its excellent efficiency achieved by the internal synchronous rectifier, making the buck an ideal green replacement for large power consuming linear regulator. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

Each of the 2 LDOs is low-dropout regulator that delivers a maximum current of 1A individual output. Typical dropout voltage at 1A load current is 1.3V. The output accuracy of each channel is set within 2% by trimming.

Typical LDO output voltage: VO1=3.3V, VO2=1.8V. Other fixed voltage (e.g 1.2V, 1.8V, 2.5V, 3.3V, 5V) or adjustable output also can be customized on command.

The LDO offers thermal shut down and current limit functions to ensure reliability of device and power system.

BL8082 is available in lead (Pb)-free DFN3X3-12 (with 2 exposed pads for heat dissipation) package.

FEATURES

BUCK

- High Efficiency : Up to 97%
- Capable of Delivering 1.2A
- 1.5MHz Switching Frequency
- No External Schottky Diode Needed
- Low dropout 100% Duty operation
- Internal Compensation and Soft-Start
- Current Mode control
- 0.6V Reference for Low Output voltages
- Logic Control Shutdown (IQ<1uA)
- Thermal shutdown, UVLO and OVP

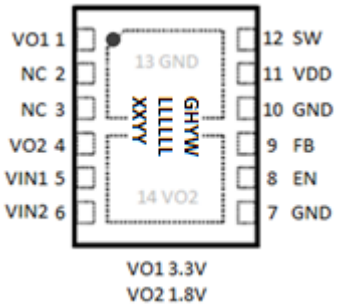
LDO

- Maximum output current for each channel is 1A
- Range of operation input voltage: Max 12V
- Standby current of each output: 2mA (typ.)
- Line regulation: 0.1%/V (typ.)
- Load regulation: 10mV (typ.)
- Compatible with tantalum capacitor, electrolytic capacitor and MLCC.

APPLICATIONS

- Power Management for Computer Mother Board, Graphic Card
- LCD Monitor and LCD TV
- DVD Decode Board
- ADSL Modem
- Set top boxes
- Post Regulators for Switching Supplies Cellular phones

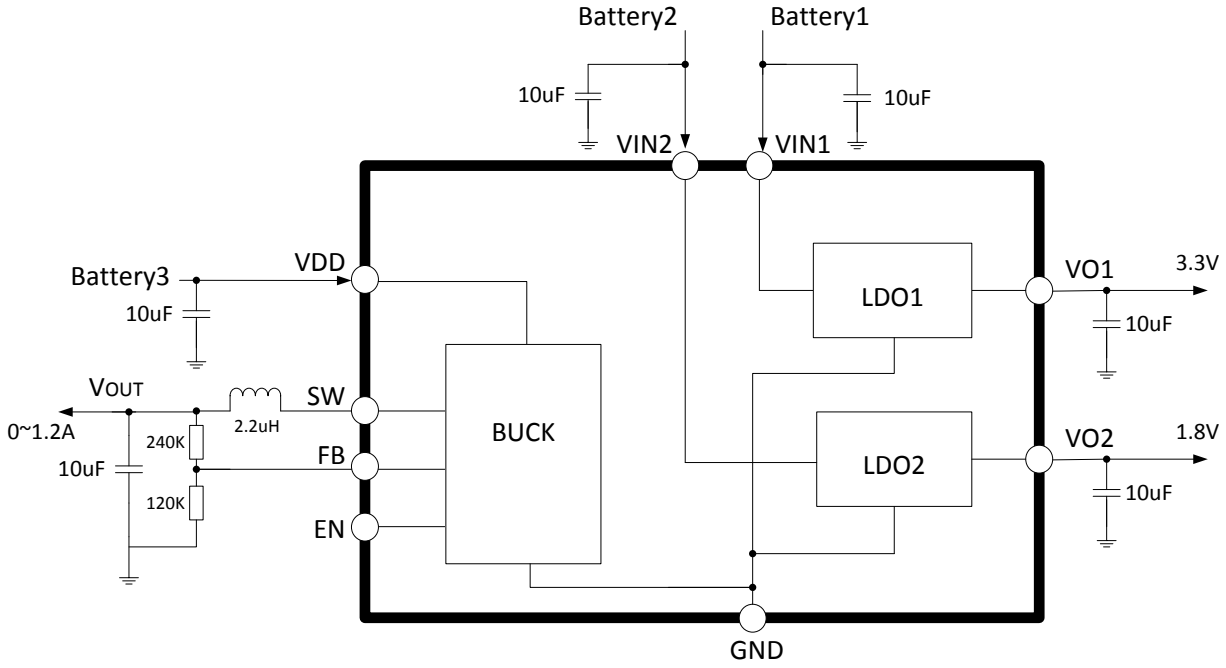
PIN OUT & MARKING



VO1 3.3V
VO2 1.8V

GH: Product Code
YW: Year & Week
LLLLLL: Lot No.
XXYY: VO1&VO2 Output Voltage
e.g. 18=1.8V 33=3.3V
AD= adjustable output

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATING

Parameter		Value
Max Input Voltage (BUCK)		8V
Max Input Voltage (LDO)		12V
Max Operating Junction Temperature(Tj)		125°C
Ambient Temperature(Ta)		-40°C – 85°C
Maximum Power Dissipation	DFN3X3-12	2W
Package Thermal Resistance (θjc)		13°C / W
Package Thermal Resistance (θjA)		60°C / W
Storage Temperature(Ts)		-40°C - 150°C
Lead Temperature & Time		260°C, 10S

Note: *Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.*

ORDERING INFORMATION

PART No.	PACKAGE	Tape&Reel
BL8082CKATR□□□□	DFN3X3-12	3000/Reel

Note: *□□□□: VO1&VO2 Output Voltage*

RECOMMENDED WORK CONDITIONS

Parameter	Value
Input Voltage Range (BUCK)	Max. 7V
Input Voltage Range (LDO)	Max. 12V
Operating Junction Temperature(Tj)	Max. 125°C

PIN DESCRIPTION

PIN #	NAME	DESCRIPTION	PIN #	NAME	DESCRIPTION
1	VO1	Output Pin (3.3V LDO)	8	EN	Enable Pin (Buck)
2	NC	Not Connected	9	FB	Feedback Pin (Buck)
3	NC	Not Connected	10	GND	Ground Pin
4	VO2	Output Pin (1.8V LDO)	11	VDD	Input Pin (Buck)
5	VIN1	Input Pin (3.3V LDO)	12	SW	Switch Pin (Buck)
6	VIN2	Input Pin (1.8V LDO)	13	GND	Ground Pin (Thermal PAD)
7	GND	Ground Pin	14	VO2	Output Pin (1.8V LDO) (Thermal PAD)

ELECTRICAL CHARACTERISTICS

(Vin=5V, TA=25°C)
BL8082CKATR3318

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUCK						
VDD	Input Voltage Range		2.6		7	V
Vref	Feedback Voltage	VDD=5V	0.588	0.6	0.612	V
Ifb	Feedback Leakage current			0.1	1	uA
Iq	Quiescent Current	Active, Vfb=0.65, No Switching		50		uA
		Shutdown			1	uA
LnReg	Line Regulation	VDD=2.7V to 5.5V		0.1	0.2	%/V
LdReg	Load Regulation	Iout=0.01 to 1A		0.1	0.2	%/A
Fsoc	Switching Frequency			1.5		MHz
OVP	Input over voltage lockout			6.5		V
RdsonP	PMOS Rdson			250	350	mohm
RdsonN	NMOS Rdson			150	250	mohm
Ilimit	Peak Current Limit		1.2	1.5	2	A
Inoload*		VDD=5V, Vout=3.3V, Iout=0		75		uA
Iswlk	SW Leakage Current	Vout=6V, VSW=0 or 6V, EN=0V			1	uA
Ienlk	EN Leakage Current				1	uA
Vh_en	EN Input High Voltage		1			V
Vl_en	EN Input Low Voltage				0.5	V
LDO						
VIN1	Input Voltage Range		VO1		12	V
VIN2	Input Voltage Range		VO2		12	V
VO1	Output Voltage	0≤Iout≤1A , VIN1=4.7V	3.234	3.3	3.366	V
VO2	Output Voltage	0≤Iout≤1A , VIN2=3.2V	1.764	1.8	1.836	V
LNR	Line Regulation	Iout=10mA, VO+1.4V≤VIN≤12V		0.15	0.3	%/V
ΔVout	Load Regulation	VIN=VO+1.4V, 10mA≤Iout≤1A		20	40	mV
Vdrop	Dropout Voltage	Iout=100mA		1.23	1.3	V
		Iout=1A		1.3	1.4	V
Ilimit	Current Limit		1			A
Iq	Quiescent Current	VIN =12V (LDO1 or LDO2)		1.5	3	mA
ΔV/ΔT	Temperature coefficient			±100		ppm

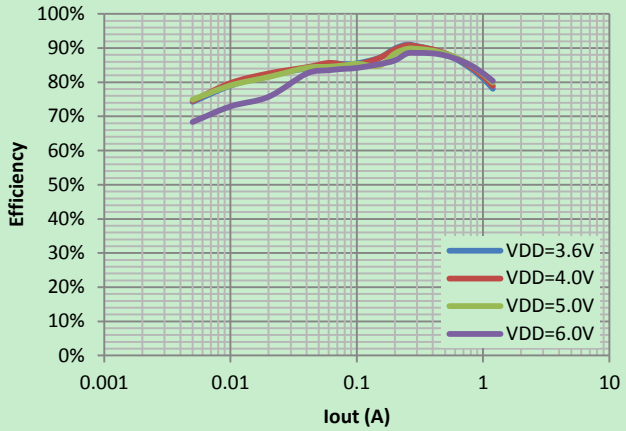
Note: **When Buck Dutycycle >80%, Inoload will increase. e.g. VDD=3.6V/Vout=3.3V, Inoload=1mA.*

ELECTRICAL PERFORMANCE

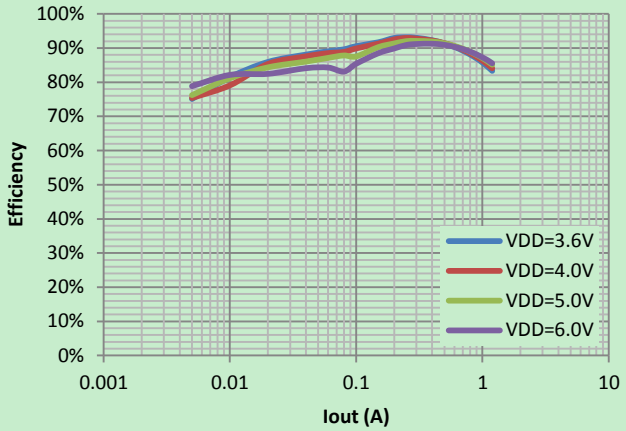
Tested under TA=25°C, unless otherwise specified

BUCK

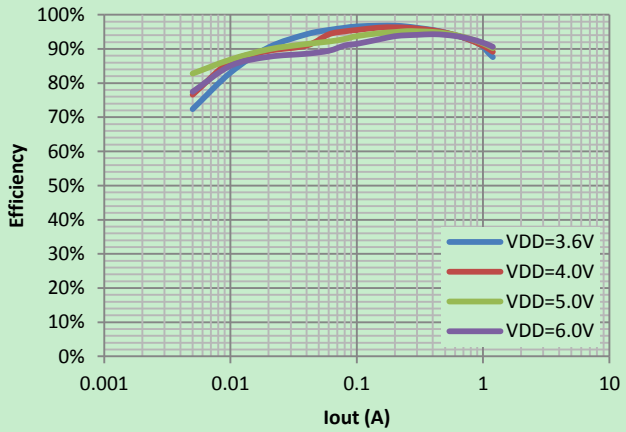
Efficiency vs. Output Current
(Vout=1.2V)



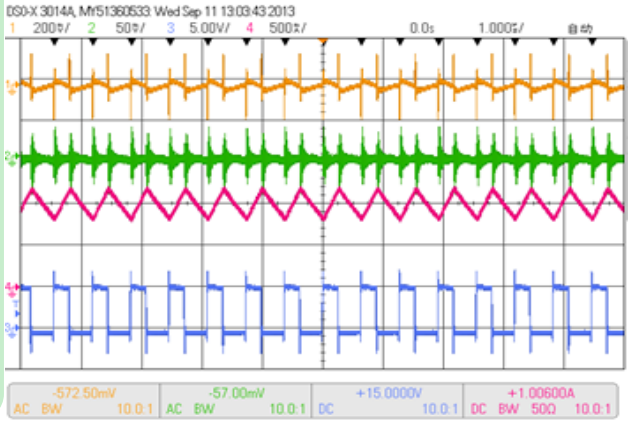
Efficiency vs. Output Current
(Vout=1.8V)



Efficiency vs. Output Current
(Vout=3.3V)

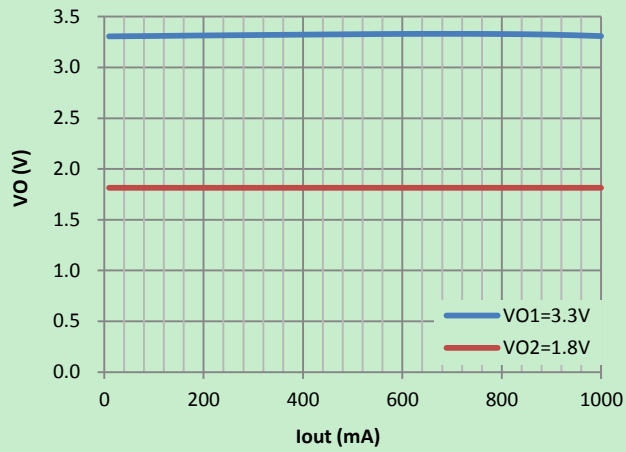


Output Ripple and SW at 1A load
VDD=5V / Vout=1.8V
Ch1—VDD, Ch2—Vout, Ch3—Vsw

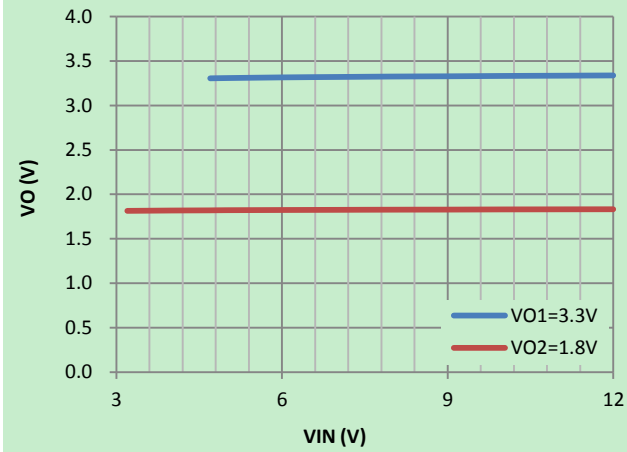


LDO

Load Regulation



Line Regulation



DETAILED DESCRIPTION

BUCK

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET of 1.5A(typ). When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. The buck utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to 1.5A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

The buck has a internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the l soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If VIN drops below 2.5V, the UVLO circuit inhibits switching. Once VIN rises above 2.6V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Setting Output Voltages

Output voltages are set by external resistors. The FB_ threshold is 0.6V.

RTOP = RBOTTOM[(VOUT / 0.6) - 1]

Input Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

VRIPPLE = IL(PEAK)[1 / (2π x fOSC x COUT)]

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:
VRIPPLE(ESR) = IL(PEAK) x ESR

LDO

The device has build-in modules including start-up circuit, bias circuit, bandgap, thermal shutdown, current limit, power transistors and driver circuit. Thermal shut down and current limit functions ensure reliability of device and power system.

The bandgap module provides stable reference voltage whose temperature coefficient is compensated by careful design considerations. The temperature coefficient is under 100 ppm/°C. The accuracy of output voltage is guaranteed by trimming technique.

Package input/output pin configuration can be customized on demand (i.e both output can share one input to save one input capacitor and corresponding PCB real estate).

THERMAL CONSIDERATIONS

Thermal consideration has to be taken account into to ensure proper function of the device. Power dissipation of BL8082 can be calculated as

LDO1 Power Dissipation = (VIN1-VO1)×IO1

LDO2 Power Dissipation = (VIN2-VO2)×IO2

BUCK Power Dissipation = VIN×IIN×10%

Total Power Dissipation = LDO1 Power Dissipation + LDO2 Power Dissipation + BUCK Power Dissipation

For proper function and safe operation of the device, LDO1 power dissipation is recommended to

be limited within 1W, LDO2 power dissipation is recommended to be limited within 1W, and total power dissipation is recommended to be limited within 2W. Due to the overall power consumption and heat of the chip, the individual pathway may not reach the maximum current due to temperature protection.

APPLICATION INFORMATION

Layout is critical to achieve clean and stable operation. The switching power stage and heat dissipation requires particular attention. Follow these guidelines for good PC board layout:

1) Place decoupling capacitors as close to the IC as possible
2) Connect input and output capacitors to the same power ground node with a star ground configuration then to IC ground.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (CIN to VIN and CIN to GND) short. Avoid vias in the switching paths.
4) If possible, connect VIN1, VO1, VIN2, VO2, VIN, SW, and GND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability. The proposed VIN1 and VO1 copper clad area of over 200 square mm (2 oz thickness).
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas.

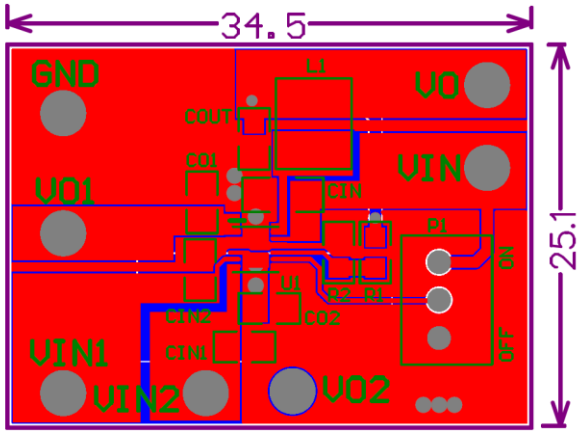
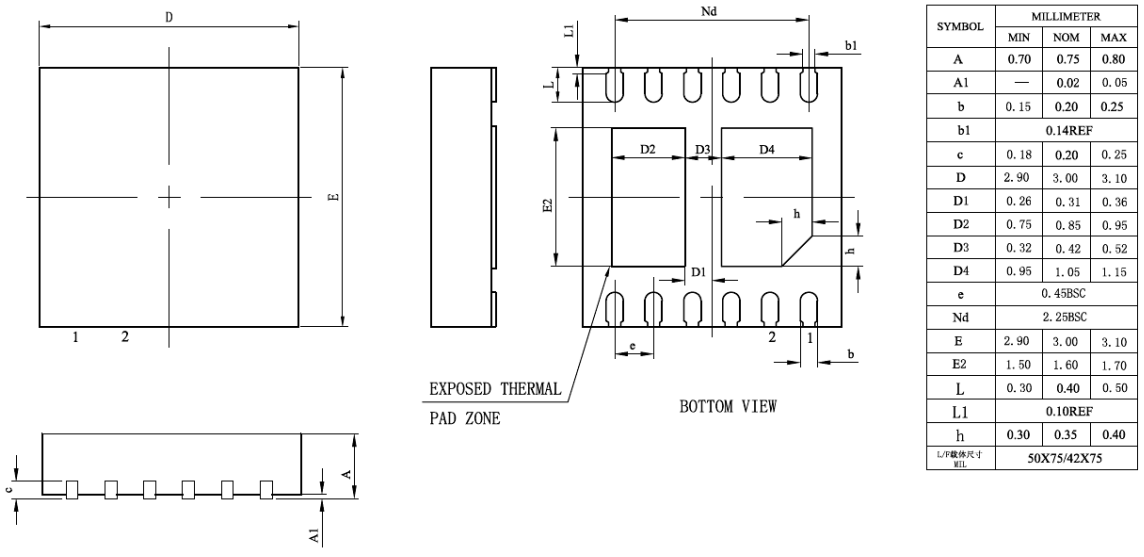


Fig1. DEMO PCB (Unit:mm)

PACKAGE OUTLINE

Package	DFN3X3-12	Devices per reel	3000	Unit	mm

Package specification：



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D1	0.26	0.31	0.36
D2	0.75	0.85	0.95
D3	0.32	0.42	0.52
D4	0.95	1.05	1.15
e	0.45BSC		
Nd	2.25BSC		
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.30	0.40	0.50
L1	0.10REF		
h	0.30	0.35	0.40
L/F载体尺寸 MIL	50X75/42X75		